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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/871,577

05/31/2001

Eyal Assa

71426

3460

22242

7590

02/08/2005

FITCH EVEN TABIN AND FLANNERY
120 SOUTH LA SALLE STREET
SUITE 1600
CHICAGO, IL 60603-3406

EXAMINER

KADING, JOSHUA A

ART UNIT

PAPER NUMBER

2661

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/871,577	Applicant(s) ASSA ET AL.	
	Examiner Joshua Kading	Art Unit 2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☒ Claim(s) 5-8, 13-16, and 22-26 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 October 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3-7-02</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Drawings

Figures 1, 2a, 2b, 3, and 4a should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected
5 drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office
10 action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 5-8, 13-16, and 22-26 are objected to because of the following informalities:

15 Each of the above claims discloses the use of an "ATM platform." Since applicant is not entirely clear on what exactly an "ATM platform" is (as required by MPEP 2106.II.(c)), it is recommended (as assumed from applicant's specification) that every instance of the term "platform" be changed to --network-- or --device-- or --system-- to more accurately and clearly disclose applicant's invention.

20 Appropriate correction is required.

Claim Rejections - 35 USC § 102

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

5 (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10 Claims 17, 19, 22, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. U.S. Patent 6,504,824 B1 (Tanaka).

15 Regarding claim 17, Tanaka discloses, "in an Asynchronous Transfer Mode (ATM) node equipment, having at least one output port and a buffer associated with each output port, the node being operative to transmit a plurality of input packet streams, according to a packet communication protocol, to any of the buffers (figures 6 and 8 where the data of figure 8 is transmitted through the system of figure 6), whereby
20 each packet is transmitted as a series of data cells, cells corresponding to different packet streams being mutually interleaved (figure 8) -- a traffic management method, comprising, with respect to any of the buffers: (i) ensuring that, while accepting input cells, the buffer has enough available capacity to store data of complete packets belonging to a substantial proportion of the input streams (figure 6 where the buffer 2
25 has a threshold that once reached will prevent more data from being stored as read in col. 1, lines 50-54); (ii) discarding all input cells as long as the buffer's available capacity falls short of enabling step (i) (col. 1, lines 58-65)."

Regarding claim 22, Tanaka discloses, "an Asynchronous Transfer Mode (ATM) node platform having at least one output port and being operative to transmit a plurality of input packet streams, according to a packet communication protocol, to any of the
5 ports (figures 6 and 8 where the data of figure 8 is transmitted through the system of figure 6), whereby each packet is transmitted as a series of data cells, cells corresponding to different packet streams being mutually interleaved (figure 8), the platform comprising a buffer (figure 6, element 2), associated with any of the output ports and being operative to accept input cells only while having enough available
10 capacity to store data of complete packets belonging to a substantial number of input streams and to discard input cells otherwise (col. 1, lines 50-65)."

Regarding claims 19 and 25, Tanaka discloses the network and platform of claims 17 and 22 respectively. Tanaka further discloses, "wherein the packet
15 communication protocol is an Internet Protocol (IP) (figure 8)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

20 (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
25

Claims 13, 16, 20, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al in view of applicant's admitted prior art (AAPA).

Regarding claim 13, Tanaka discloses, "an Asynchronous Transfer Mode (ATM) platform, having at least one output port and being operative to transmit data according to a packet communication protocol (figures 6 and 8 where the data of figure 8 is transmitted through the system of figure 6); the data includes packets and each packet is transmitted as a series of data cells, each cell including a Virtual Path Indicator (VPI) and being routable to any of the output ports (figure 8 and col. 2, lines 18-22), and the platform is further operative to manage the flow of cells to at least one of the output ports, it being a managed port, so that, over any period of time during which the number of cells routed to the port exceeds the number of cells transmittable therefrom, the proportion of complete packets transmitted is substantially greater than if the flow were not thus managed (col. 1, lines 50-65 where although there are packets that are discarded, had there been no management, i.e. no FIFO, then a lot more packets would be lost due to the fact that there would no longer be a buffer available for storage)."

However, Tanaka lacks what AAPA discloses, "at least some of the cells being routable according to their respective VPIs only (specification, page 2, lines 12-15)."

It would have been obvious to one of ordinary skill in the art at the time of invention to include the VPI only routing for the purpose of further routing the cells according to the only routing information available, the VPI. The motivation for further routing cells is to complete transmission.

Regarding claim 16, Tanaka and AAPA disclose the platform of claim 13.

However, AAPA lacks what Tanaka further discloses, "wherein the packet communication protocol is an Internet Protocol (IP) (figure 8)." It would have been

5 obvious to one of ordinary skill in the art at the time of invention to include the IP communication protocol for the same reasons and motivation as in claim 13.

Regarding claims 20 and 26, Tanaka discloses the network of claim 17 and platform of claim 22. However, Tanaka lacks what AAPA discloses, "wherein each data
10 cell includes a Virtual Path Indicator (VPI) and wherein any data cell is routed according to its VPI only (specification, page 2, lines 12-15)." It would have been obvious to one of ordinary skill in the art at the time of invention to include the VPI only routing for the purpose of further routing the cells according to the only routing information available, the VPI. The motivation for further routing cells is to complete transmission.

15

Claims 1, 2, 4-6, 8-10, 12, 18, 21, 23, 24, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. in view of U.S. Patent 5,506,967 Barajas et al. (Barajas).

20

Regarding claims 1, 5, and 9 Tanaka discloses the networks of claims 1 and 9, and the platform of claim 5. Tanaka further discloses, "An Asynchronous Transfer Mode (ATM) network of nodes operative to transmit data according to a packet

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communication protocol (figures 6 and 8 where the data of figure 8 is transmitted through the system of figure 6); the data includes packets and each packet is transmitted as a series of data cells (figure 8); at least one of said nodes comprises one or more buffers for storing data cells routed to them and designated to be transmitted from the node (figure 6, element 2); and any of said buffers is operative to perform at least the following while in an Absorbing State, to receive and store any cell routed to it and, further, when its fill level reaches a maximum level to switch to a blocking state (col. 1, lines 50-65 whereby not storing the data in the FIFO, it is blocked)..."

However, Tanaka lacks what Barajas discloses, "while in said blocking state, to refrain from receiving and storing any cell and, further, when its fill level falls below a hysteresis level, lower than said maximum level, to switch to said absorbing state (col. 7, lines 28-29 and col. 8, lines 57-65 where although the components of Barajas are not explicitly described as working in an ATM environment, one of ordinary skill would recognize that the invention of Barajas would be applicable to any buffered type computer system, such as one in an ATM environment)."

It would have been obvious to one of ordinary skill in the art at the time of invention to include the hysteresis level in the blocking state for the purpose of allowing the buffer to clear or flush out a substantial amount of data. The motivation for clearing the buffer is so that there will be adequate space for the storage of data and the problem of overfill will have been solved for that moment.

Regarding claims 2, 6, and 10, Tanaka and Barajas disclose the networks of claims 1 and 9, and the platform of claim 5. However, Barajas lacks what Tanaka further discloses, "wherein the packet communication protocol is an Internet Protocol (IP) (figure 8)." It would have been obvious to one of ordinary skill in the art at the time of invention to include the IP communication protocol for the same reasons and motivation as in claims 1, 5, and 9.

Regarding claims 4, 8, 12, 21, and 24, Tanaka disclose the network and platform of claims 17 and 22 respectively, and the networks of claims 1 and 9, and the platform of claim 5. However, Tanaka lacks what Barajas further discloses, "wherein, at any node and for any buffer, said hysteresis level is determined according to some measure of the rate of total cells traffic routed to the buffer (col. 10, lines 59-col. 11, lines 1-3)." It would have been obvious to one of ordinary skill in the art at the time of invention to include the hysteresis level for the purpose of allowing the buffer to clear or flush out a substantial amount of data. The motivation for clearing the buffer is so that there will be adequate space for the storage of data and the problem of overfill will have been solved for that moment.

Regarding claims 18 and 23, Tanaka discloses the network of claim 17 and the platform of claim 22. Tanaka further discloses, "wherein said buffer is further operative to perform at least the following while in an absorbing state, to receive and store any cell routed to it and, further, when its fill level reaches a maximum level, to switch to a

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blocking state (col. 1, lines 50-65 whereby not storing the data in the FIFO, it is blocked)..."

However, Tanaka lacks what Barajas discloses, "while in said blocking state, to refrain from receiving and storing any cell and, further, when its fill level falls below a hysteresis level, lower than said maximum level, to switch to said absorbing state (col. 7, lines 28-29 and col. 8, lines 57-65 where although the components of Barajas are not explicitly described as working in an ATM environment, one of ordinary skill would recognize that the invention of Barajas would be applicable to any buffered type computer system, such as one in an ATM environment)."

It would have been obvious to one of ordinary skill in the art at the time of invention to include the hysteresis level in the blocking state for the purpose of allowing the buffer to clear or flush out a substantial amount of data. The motivation for clearing the buffer is so that there will be adequate space for the storage of data and the problem of overfill will have been solved for that moment.

Regarding claims 27 and 28, Tanaka discloses, "in an Asynchronous Transfer Mode (ATM) network of nodes operative to transmit data according to a packet communication protocol (figures 6 and 8 where the data of figure 8 is transmitted through the system of figure 6), whereby the data includes packets and each packet is transmitted as a series of data cells (figure 8), the network including, at one or more nodes, at least one buffer for storing data cells routed to them and designated to be transmitted from the node (figure 6, element 2)...the buffer, while in an absorbing state,

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to receive and store any cell routed to it and, further, when the buffer's fill level reaches a maximum level, to switch to a blocking state (col. 1, lines 50-65 whereby not storing the data in the FIFO, it is blocked)..."

However, Tanaka lacks what Barajas discloses, "-- a traffic management

5 computer program product comprising a computer useable medium having computer readable program code embodied therein, the computer program product comprising...computer readable program code for" the absorbing state (col. 1, lines 13-30), and "and computer readable program code for causing the computer to cause the buffer, while in said blocking state, to refrain from receiving and storing any cell and, 10 further, when the buffer's fill level falls below a hysteresis level, to switch to said absorbing state (col. 7, lines 28-29 and col. 8, lines 57-65 where although the components of Barajas are not explicitly described as working in an ATM environment, one of ordinary skill would recognize that the invention of Barajas would be applicable to any buffered type computer system, such as one in an ATM environment)."

15 It would have been obvious to one of ordinary skill in the art at the time of invention to include the computer program (which is a machine that instructs a component of the computer system to do something) and hysteresis level in the blocking state for the purpose of allowing the buffer to clear or flush out a substantial amount of data. The motivation for clearing the buffer is so that there will be adequate 20 space for the storage of data and the problem of overflow will have been solved for that moment.

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Claims 3, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. and Barajas et al. as applied to claims 1, 8, and 9 above, and further in view of applicant's admitted prior art (AAPA).

Regarding claims 3, 7, and 11, Tanaka and Barajas disclose the networks of
5 claims 1 and 9, and the platform of claim 5. However, Tanaka and Barajas lack what AAPA discloses, "wherein each data cell includes a Virtual Path Indicator (VPI) and wherein any data cell is routed according to its VPI only (specification, page 2, lines 12-15)." It would have been obvious to one of ordinary skill in the art at the time of invention to include the VPI only routing for the purpose of further routing the cells according to
10 the only routing information available, the VPI. The motivation for further routing cells is to complete transmission.

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. and AAPA as applied to claim 13 above, and further in view of
15 Barajas et al.

Regarding claim 14, Tanaka and AAPA disclose the platform of claim 13. Tanaka further discloses, "a buffer, associated with any of said managed ports and serving to store cells designated to be transmitted therefrom, said buffer being operative to
20 perform at least the following while in an absorbing state, to receive and store any cell routed to it and, further, when its fill level reaches a maximum level, to switch to a

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blocking state (col. 1, lines 50-65 whereby not storing the data in the FIFO, it is blocked)..."

However, Tanaka and AAPA lack what Barajas discloses, "while in said blocking state, to refrain from receiving and storing any cell and, further, when its fill level falls
5 below a hysteresis level, lower than said maximum level, to switch to said absorbing state (col. 7, lines 28-29 and col. 8, lines 57-65 where although the components of Barajas are not explicitly described as working in an ATM environment, one of ordinary skill would recognize that the invention of Barajas would be applicable to any buffered type computer system, such as one in an ATM environment)."

10 It would have been obvious to one of ordinary skill in the art at the time of invention to include the computer program (which is a machine that instructs a component of the computer system to do something) and hysteresis level in the blocking state for the purpose of allowing the buffer to clear or flush out a substantial amount of data. The motivation for clearing the buffer is so that there will be adequate
15 space for the storage of data and the problem of overfill will have been solved for that moment.

Regarding claim 15, Tanaka and AAPA disclose the platform of claim 13.

However, Tanaka and AAPA lack what Barajas discloses, "wherein said hysteresis level
20 is determined according to some measure of the rate of total cells traffic routed to the buffer (col. 10, lines 59-col. 11, lines 1-3)." It would have been obvious to one of ordinary skill in the art at the time of invention to include the hysteresis level for the

purpose of allowing the buffer to clear or flush out a substantial amount of data. The motivation for clearing the buffer is so that there will be adequate space for the storage of data and the problem of overfill will have been solved for that moment.

5

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,452,915 B1 Jorgensen discloses a ATM network capable of IP packet transport and the use of only the VPI to route cells.

10

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Kading whose telephone number is (571) 272-3070. The examiner can normally be reached on M-F: 8:30AM-5PM.

15

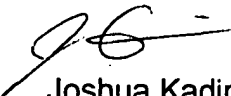
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

20

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

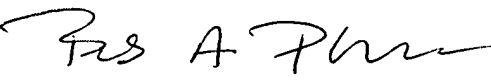
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Joshua Kading
Examiner
Art Unit 2661

February 4, 2005



BOB PHUNKULH
PRIMARY EXAMINER